The following claims are presented for examination:

1.-16. (previously canceled)

17.-27 (canceled)

28. (new) An apparatus comprising:

circuitry for receiving a source clock signal from an external device and for receiving data from said external device at a rate equal to the frequency of said source clock signal; and

a function clock generator that generates a function clock signal from said source clock signal, wherein said function clock signal alternates between having the same frequency as said source clock signal and twice the frequency as said source clock signal.

29. (new) The apparatus of claim 28 wherein said function clock signal comprises a plurality of edges, wherein said source clock signal comprises a plurality of edges, and wherein the edges of said function clock signals only occur when an edge of said source clock signal occurs.

30. (new) The apparatus of claim 28 further comprising a program counter that is incremented by said function clock signal.

31. (new) The apparatus of claim 28 futher comprising:

a memory for storing an instruction at each of a plurality of addresses;

a program counter for providing said plurality of addresses into said memory and that is incremented by said function clock signal; and

an instruction decoder for decoding an instruction from said memory that instructs said function clock generator to change the frequency of said function clock signal.

32. (new) The apparatus of claim 31 wherein the phase of said source clock signal and the phase of said function clock signal are the same when they have the same frequency.

33. (new) The apparatus of claim 31 wherein the phase of said source clock signal and the phase of said function clock signal are 180° out of phase when they have the same frequency.

---

34. (new) An apparatus comprising:

circuitry for receiving a source clock signal from an external device and for transmitting data to said external device at a rate equal to the frequency of said source clock signal;

a function clock generator that generates a function clock signal from said source clock signal, wherein said function clock signal alternates between having the same frequency as said source clock signal and twice the frequency as said source clock signal.

35. (new) The apparatus of claim 34 wherein said function clock signal comprises a plurality of edges, wherein said source clock signal comprises a plurality of edges, and wherein the edges of said function clock signals only occur when an edge of said source clock signal occurs.

36. (new) The apparatus of claim 34 further comprising a program counter that is incremented by said function clock signal.

37. (new) The apparatus of claim 34 futher comprising:

a memory for storing an instruction at each of a plurality of addresses;

a program counter for providing said plurality of addresses into said memory and that is incremented by said function clock signal; and

an instruction decoder for decoding an instruction from said memory that instructs said function clock generator to change the frequency of said function clock signal.

38. (new) The apparatus of claim 37 wherein the phase of said source clock signal and the phase of said function clock signal are the same.

39. (new) The apparatus of claim 37 wherein the phase of said source clock signal and the phase of said function clock signal are 180° out of phase.